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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/762,981	05/09/2001	Andrea Olgiati	B-4089PCT	1339

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/762,981	OLGIATI ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14,15,17 and 18* is/are rejected.

7)☒ Claim(s) *13 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-12, 14, 15, 17, and 18 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Stein US Patent 5,708,830, cited as a prior art reference in the IDS filed by Applicant on January 14, 2001 (herein referred to as Stein).

3. Referring to claim 1, Stein has taught a computer system, comprising:

a. a first processor (host processor, column 2, lines 45-49);

b. a second processor for use as a coprocessor to the first processor (Figures 1 and 2);

c. a coprocessor controller (Figure 1, element 14, column 7, lines 39-45);

d. a memory (column 2, lines 45-49, Figure 1, main memory of the host processor, via element PCDATA, and Figure 2, element 28); and

e. a decoupling element (Figure 1, elements 6, 18, 14, 4, 10 and 12);

f. wherein computations are passed to the second processor from the first processor through the decoupling element, such that the second processor executes computations passed from the first processor through the decoupling element (abstract, column 1, line 54-column 2, line 36), wherein the second processor receives data from and writes data to the memory (Figure 1, via element PCDATA), and wherein the coprocessor controller

controls the activity of the second processor to ensure execution of the second processor is correctly ordered with respect to loads from memory (column 2, line 58-column 3, line 2, column 3, line 24-column 4, line 3, column 5, lines 26-62, column 7, lines 39-45), whereby the execution of computations by the second processor is decoupled from the operation of the first processor (column 1, lines 54-60, column 2, lines 27-34, column 3, lines 55-60, column 7, line 57-column 8, line 3) such that the second processor executes computations passed from the first processor through the decoupling element while the first processor is providing further instructions to the decoupling element (column 2, line 63-column 3, line 2, column 5, lines 45-47, column 6, lines 30-37, Instructions are executed while instructions and data are provided to the FIFO's.).

4. Referring to claim 2, Stein has taught a computer system as claimed in claim 1, as described above, and wherein the decoupling element is a coprocessor instruction queue, wherein computations are added to the coprocessor instruction queue by the first processor and consumed from the coprocessor instruction queue by the coprocessor (Figure 1, elements 6, 18, 14, 4, 10 and 12, column 2, line 45-column 3, line 2).

5. Referring to claim 3, Porter et al. have taught a computer system as claimed in claim 1, as described above, and wherein the decoupling element is a state machine, wherein information to provide computations to the second processor is provided to the state machine by the first processor, and computations are provided in an ordered sequence to the second processor by the state machine (Figure 1, elements 6, 18, 14, 4, 10 and 12).

6. Referring to claim 4, Stein has taught a computer system as claimed in claim 1, as described above, and wherein the decoupling element is a third processor, wherein information

to provide computations to the second processor is provided to the third processor by the first processor, and computations are provided in an ordered sequence to the second processor by the third processor (Figure 1, elements 18 and 14, column 3, line 45-column 4, line 3).

7. Referring to claim 5, Stein has taught a computer system as claimed in claim 1, as described above, and wherein the second processor is configurable (column 1, line 44-column 2, line 36, column 4, lines 25-29).

8. Referring to claim 6, Stein has taught a computer system as claimed in claim 5, as described above, and wherein the second processor is adapted to be configured in accordance with a configuration downloaded from the memory (column 1, line 44-column 2, line 36, column 4, lines 25-29).

9. Referring to claim 7, Stein has taught a computer system as claimed in claim 1, as described above, and wherein the first processor is able to switch tasks during execution of computations by the second processor (column 1, lines 54-60, column 2, lines 27-34, column 3, lines 55-60, column 7, line 57-column 8, line 3).

10. Referring to claim 8, Stein has taught a computer system as claimed in claim 1, as described above, and further comprising a buffer memory from which the second processor loads data and to which the second processor stores data, wherein the buffer memory is adapted to load data from the memory and store data to the memory (Figure 1, elements 4, 6, 10,12, and Figure 2, element 24.).

11. Referring to claim 9, Stein has taught a computer system as claimed in claim 8, as described above, and wherein the memory is dynamic random access memory (Figure 2, element

28), and the buffer memory is adapted to load data from, or store data to, the buffer memory in bursts (column 2, line 46-column 3, line 2).

12. Referring to claim 10, Stein has taught a computer system as claimed in claim 8, as described above, and further comprising a second decoupling element, wherein memory instructions relating to movement of data between the buffer memory and the memory are passed to the buffer memory from the first processor through the second decoupling element, such that the buffer memory consumes instructions derived from the first processor through the second decoupling element, whereby the processing of memory instructions by the buffer memory is decoupled from the operation of the first processor (Figure 1, elements 18 and 16, 18, 14, 4, 10 and 12).

13. Referring to claim 11, Stein has taught the computer system as claimed in claim 10, as described above, and wherein the second decoupling element is a buffer memory instruction queue, wherein memory instructions are added to the buffer memory instruction queue by the first processor and consumed from the buffer memory instruction queue by the buffer memory (Figure 1, elements 6, 18, 14, 4, 10, and 12, column 2, line 45-column 3, line 2).

14. Referring to claim 12, Stein has taught a computer system as claimed in claim 10, as described above, and wherein the second decoupling element is a state machine (Figure 1, elements 2, 6, 18, 14, 4, 10, and 12), wherein information to provide memory instructions to the buffer memory is provided to the state machine by the first processor, and memory instructions are provided in an ordered sequence to the buffer memory by the state machine (column 2, line 58-column 3, line 2, column 3, line 24-column4, line 3, column 5, lines 26-62, column 7, lines 39-45).

15. Referring to claim 14, Stein has taught a computer system as claimed in claim 8, as described above, and further comprising a synchronisation mechanism to synchronise transfer of data between the buffer memory and the memory with execution of computations by the second processor (column 8, lines 39-47).

16. Referring to claim 15, Stein has taught a computer system as claimed in claim 14, as described above, and wherein the synchronisation mechanism is adapted to block execution of computations by the second processor on data which has not yet been loaded to the buffer memory from the memory, and is adapted to block execution of memory instructions for storage of data from the buffer memory to the memory where relevant computations have not yet been executed by the second processor (column 8, lines 39-47).

17. Referring to claim 17, Stein has taught a computer system as claimed in claim 1, as described above, and wherein the first processor is the central processing unit of a computer device (host processor, column 2, lines 45-49).

18. Referring to claim 18, Stein has taught a method of operating a computer system, comprising:

a. providing code for execution by a first processor and a second processor acting as coprocessor to the first processor (abstract, column1, lines 39-60, the host processor is the first processor, column 2, lines 45-49, Figures 1 and 2 illustrate the second processor.);

b. identification of a part of the code as providing a task to be carried out by the second processor (abstract, column1, lines 39-60);

c. passing information defining the task from the first processor to a decoupling element (Instructions are passed from the host to the decoupling elements, 2, 6, 18, 14, 4, 10 and 12, via PCADDR and PCDATA);

d. passing instructions derived from said information from the decoupling element to the second processor and executing said instructions on the second processor (abstract, column1, line 39-column 2, line 37), wherein the processing of said instructions by the second processor is decoupled from the operation of the first processor (column 1, lines 54-60, column 2, lines 27-34, column 2, line 63-column 3, line 2, column 3, lines 55-60, column 7, line 57-column 8, line 3) such that the second processor executes said instructions passed from the decoupling element while the first processor passes further information defining the task to the decoupling element (column 2, line 63-column 3, line 2, column 5, lines 45-47, column 6, lines 30-37, Instructions are executed while instructions and data are provided to the FIFO's.).

Response to Arguments

19. Applicant's arguments with respect to claims 1-12, 14, 15, 17, and 18 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

20. Claims 13 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

22. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

2/2/06

HENRY W. H. TSAI
PRIMARY EXAMINER